A Low-Power Temperature and Process Insensitive CMOS Power Management Unit

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***Abstract*—A Power Management Unit aimed for applications requiring low consumption and area efficiency is introduced in this work. Its main goal is to deliver the desired voltage and current outputs to be used from the other circuits of the system. In this particular topology a power consumption of 591 nW is achieved along with PSRR of 25.15 dB in worst case and a dropout voltage of 0.3 V. This work is supposed to serve as a proof of concept for very low consumption design of Power Management Units and may be included in architectures that integrate advanced features, like DC-DC converters, Pulse Width Modulation mode along with complex digital control part. The proposed system is designed and simulated using the Cadence IC Suite in a TSMC 90nm CMOS process.**

***Index Terms*—VLSI, Low Power design, Power Management Unit, Low-Dropout Regulator, Bandgap Reference Circuit**

I. Introduction

Integrated circuits (ICs) have witnessed an unprecedented evolution, marked by a pursuit of smaller form factors, increased functionality, and energy efficiency. This evolution has led to the widespread integration of electronic devices, with applications spanning from wearables and Internet of Things (IoT) devices to medical implants and mobile computing. These applications share a common demand; the need for extended battery life, reduced heat dissipation, and, above all, efficient power management [1]. A Power Management Unit (PMU) is a complex electronic circuit designed to efficiently control and manage the distribution of power within ICs or electronic systems. Its primary function is to ensure that the various components of a system receive the required supply voltage and current levels while optimizing power consumption. [2]

This work presents a comprehensive exploration of a PMU design. It is built to meet the stringent power management requirements of low-power applications with the primary design specification being the power consumption of the circuit and its building blocks. However various approaches were implemented and tested in order not only to minimize the power consumption, but at the same time to achieve exceptional results regarding all the main specifications commonly examined when designing a PMU. Such parameters are the driving capability of the PMU, the Power Supply Rejection Ratio (PSRR), the noise and stability performance, the response of the circuit during start-up and other design aspects presented and analyzed in Section IV. Moreover of high significance during the design flow was the performance of the proposed PMU over Process-Voltage-Temperature (PVT) corners variation. The circuit presented in this work is designed to achieve descent performance across all corners without significantly affecting its proper operation. Numerous simulations have been executed, including corner cases, to evaluate the performance and robustness of the proposed PMU.

The rest of this work is organized in the following manner. Section II provides a description of the system-level architecture of the proposed PMU. In Section III the main building blocks are presented and analyzed. The implemented layout along with the results of the conducted simulations are summarized and discussed in Section IV. Finally, Section V indicates some concluding remarks.

II. PMU's Architecture

The architecture of the proposed PMU is presented in this Section. It is designed to efficiently regulate and distribute power within a system. As shown in Fig. 1, it comprises a Bandgap Reference Circuit (BGR), a Low-Dropout Regulator (LDO), a Constant Transconductance (g_m) Circuit, a current bleeder integrated within the LDO, and an R-C low-pass filter. This architecture serves a critical role in enhancing the stability and reliability of the power supply.

The BGR acts as a stable voltage reference, providing a consistent baseline for the entire system [3]. The LDO, with its low dropout voltage, ensures a minimal voltage differential between its input and output, facilitating precise voltage regulation [2], [4]. The inclusion of a constant-g_m circuit contributes to consistent transconductance and current generation across varying operational conditions, optimizing the overall performance [5]. The integrated current bleeder within the LDO adds a dynamic element, enabling efficient power dissipation assuring for stability when necessary [2]. Finally, the R-C filter placed between the BGR and the LDO attenuates high-frequency noise, guaranteeing a clean and stable output. Each component in this power management unit plays a distinct and essential role, collectively contributing to the system's robustness and energy efficiency.

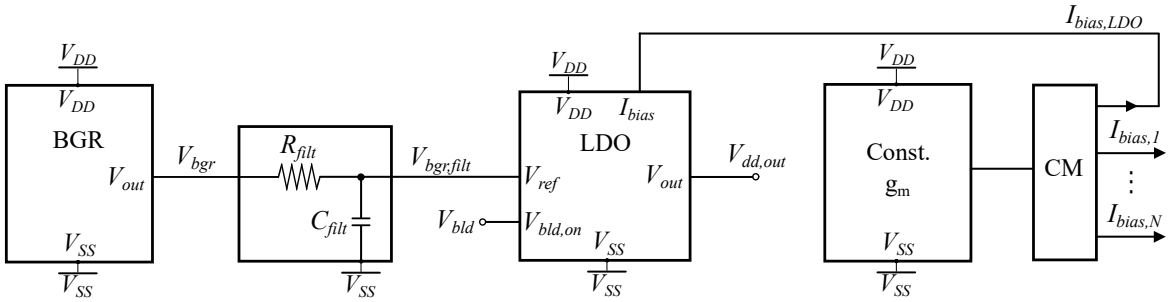

Fig. 1: Architecture of the designed PMU with its main building blocks.

III. Basic Building Blocks

In this Section the fundamental units that form the proposed PMU are analyzed.

A. Bandgap Reference

BGRs are structural components in ICs, providing an accurate and stable with respect to PVT variations voltage reference, crucial for the reliable operation of various electronic systems. The traditional BGRs reported in literature leverage the energy bandgap of a semiconductor to generate a constant voltage output, independent of temperature variations. To achieve this, they typically use bipolar junctions, resistors and amplifiers resulting in increased power consumption and silicon area requirements [3]. To meet the demand for low power, area, and minimum functional supply, the BGR implemented in this work, as illustrated in Fig. 2, consists of only three MOS transistors.

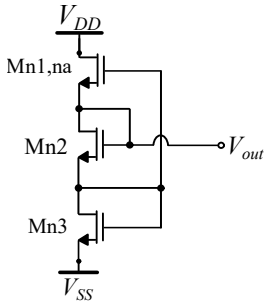

Fig. 2: The implemented BGR circuit. It consists of one native and two I/O NMOS transistors.

In this design two different device types are used; a native NMOS device for $M_{n1,na}$ and thick oxide input/output (I/O) NMOS transistors for M_{n2} and M_{n3}. Native NMOS transistors are fabricated in order that they have negative or nearly zero threshold voltage [6]. Both devices have thick gate oxides to be able to support a high V_{dd}, boosting the reliability of the circuit. Transistors M_{n2} and M_{n3} operate in the subthreshold region, in which the current equation is

$$I = \mu C_{ox} \frac{W}{L} (m-1) V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{m V_T}\right) \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (1)$$

where μ is mobility, C_{ox} is oxide capacitance, W is transistor width, L is transistor length, m is subthreshold slope factor, V_T is thermal voltage, V_{gs} is gate to source voltage, V_{th} is transistor threshold voltage, and V_{ds} is drain to source voltage [5]. The output voltage of the circuit depends mainly on i) the threshold voltages difference of the devices, ii) the thermal voltage and iii) the sizing of the devices. Threshold voltage is complementary to temperature, while the thermal voltage is proportional to absolute temperature. Adjusting the sizes of the devices appropriately, a very low Temperature Coefficient may be achieved even for the corner cases, minimizing both the temperature sensitivity and the power consumption [7]. It is worth to mention that not only native and I/O transistors are suitable for the implementation of this BGR but any two types of devices with significant threshold voltage difference. The sizes of the devices are summarized in Table I.

TABLE I: BGR Sizing (Fig. 2).

NMOS	W/L (µm/µm)	NMOS	W/L (µm/µm)
$M_{n1,na}$	12/1.2	M_{n2},M_{n3}	4/1

B. Low-Dropout Regulator

LDOs find spot in almost every modern electronic device, due to their ability to step down a DC voltage and also reject ripple from their input to their output. The designed NMOS LDO is structured as shown in Fig. 3. It is composed of an Error Amplifier (EA), that provides the necessary gain value and a large transistor - usually called pass-device - that undertakes the task of delivering current to the load of the PMU [2], [4], [5]. Despite the fact that NMOS LDOs in general have many advantages, such as low output resistance, straightforward compensation and better load regulation, their main vulnerability is the limited dropout voltage, and that is the reason why they may seem inappropriate for low-voltage applications. This is why in the implemented design a native NMOS transistor, $M_{pass,na}$, is selected to serve as pass-device. Their nearly zero threshold voltage makes them suitable for LDO designs that require a very low dropout voltage avoiding the use of Charge Pump [2]. In this work the LDO is additionally equipped with a current bleeder, formed by the resistor R_{bld} and the NMOS $M_{bld,sw}$ that operates as a switch controlled by the external voltage $V_{bld,on}$. When setting

$V_{bld,on}$ to HIGH, the bleeder operates increasing the current through pass transistor, thus assuring for the stability of the LDO in very low values of load current.

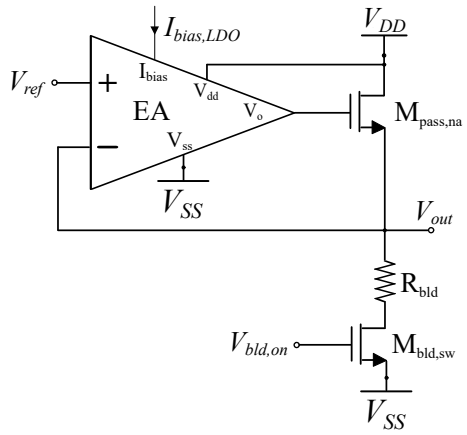

Fig. 3: The selected topology for LDO design. It consists of i) one large native NMOS pass-transistor, ii) the error amplifier and iii) the current bleeder.

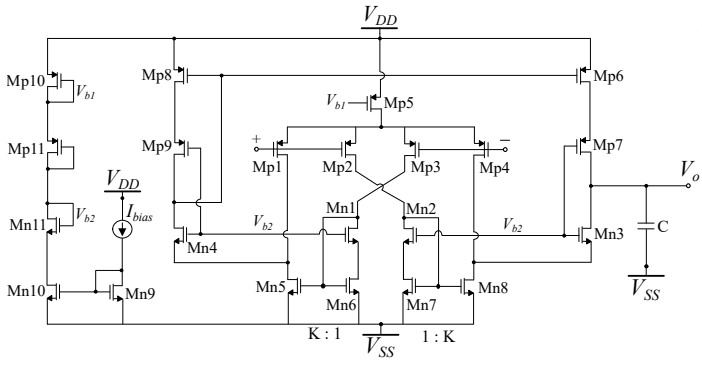

Fig. 4: The recycling folded cascode op-amp realizing the error amplifier of the LDO.

Demand for system on-chip solutions has aroused interest in LDOs, that do not need bulky off-chip capacitors in order to remain stable, also called capacitor-less LDO (CL-LDO) regulators. At the same time, folded cascode operation amplifiers, are another popular circuit in CMOS process, mostly due to its high DC gain and low noise characteristics. Taking all the above into consideration, the required EA is implemented with a recycling folded cascode operational amplifier (op-amp), in an attempt to enhance the bandwidth and the transconductance of the conventional folded cascode topology [8], [9]. The corresponding topology is depicted in Fig. 4. The transconductance and output impedance of the recycling folded cascode opamp, are respectively:

$$G_m = (1+K)g_{m_{p1}} \tag{2}$$

$$R_{out} = \left[g_{m_{p7}} r_{o_{p7}} r_{o_{p6}}\right] || \left[g_{m_{n3}} r_{o_{n3}} \left(r_{o_{n8}} || r_{o_{p4}}\right)\right] \tag{3}$$

The sizes of the devices are summarized in Table II.

TABLE II: LDO Sizing (Fig. 3,4) and R-C Filter.

NMOS	W/L (µm/µm)	PMOS	W/L (µm/µm)
M_{n1},M_{n2}	0.3/17	M_{p1}-M_{p4}	1.2/4
M_{n3}	12/2	M_{p5}	1/4
M_{n4}	14/2	M_{p6},M_{p8}	0.48/9
M_{n5},M_{n8}	0.48/17	M_{p7}	0.48/2
M_{n6},M_{n7}	0.24/17	M_{p9}	0.48/3
M_{n9}	2/0.5	M_{p10}	0.4/4
M_{n10},M_{n11}	20/4	M_{p11}	2.4/4
$M_{pass,na}$	1000/1.2	-	-
$M_{bld,sw}$	0.2/0.1	-	-
Resistors	**MΩ**	**Capacitors**	**pF**
R_{bld}	5	C	15
R_{filt}	0.05	C_{filt}	15

C. Constant Transconductance Circuit

A Constant Transconductance (g_m) circuit produces a small-signal transconductance that is a fixed fraction of a resistor value. To a first-order approach, the transistors' transconductances are independent of PVT variations [5]. In the current design, the constant g_m circuit depicted in Fig. 5, accompanied with the multiple current mirror (CM) is utilized like a current generator for the LDO's error amplifier and for any other circuit on the chip demanding a constant bias current.

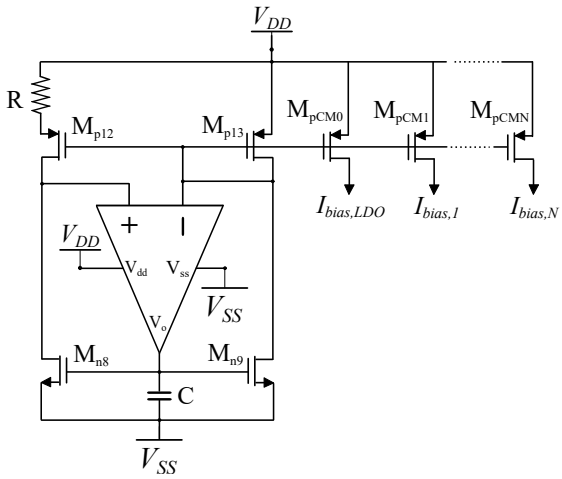

Fig. 5: The constant g_m circuit together with the current mirrors used for biasing.

Employing PMOS transistors, specifically M_{p12} and M_{p13}, effectively mitigates the body effect. The amplifier equalizes voltages at the drain terminals of the transistors, thereby minimizing the impact of finite transistor output impedance. Additionally, the amplifier decreases the impedance at the drain, diminishing the gain within the positive feedback loop and enhancing overall stability. To ensure stability within the negative feedback loop, constituted by the amplifier and common-source transistors, proper sizing of the compensation capacitor C is essential [5]. The amplifier utilizes an Ahuja compensation op-amp [10], as shown in Fig. 6.

The sizes of the devices are summarized in Table III.

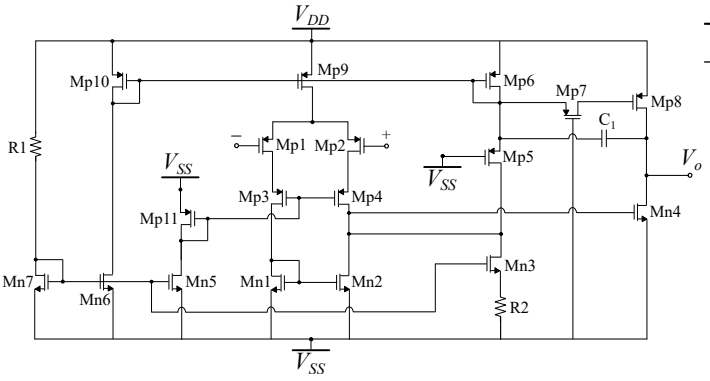

Fig. 6: The Ahuja-compensation op-amp included in the constant-g_m circuit [10].

TABLE III: Constant-g_m Sizing (Fig. 5,6).

NMOS	W/L (µm/µm)	PMOS	W/L (µm/µm)
M_{n1},M_{n2}	8/0.2	M_{p1}-M_{p4},M_{p11}	32/0.5
M_{n3}	24/0.4	M_{p5}	2/2
M_{n4}	0.8/0.2	M_{p6},M_{p8}	12/2
M_{n5}	2/0.4	M_{p7}	0.2/0.1
M_{n6},M_{n7}	4/0.4	M_{p9}	8/2
M_{n8},M_{n9}	0.12/5	M_{p12}	0.48/5
-	-	M_{p13},M_{pCM}	0.12/5
Resistors	**MΩ**	**Capacitors**	**pF**
R_1	150	C_1	5
R_2	0.1	-	-
R	5	C	10

IV. Simulation Results

In this section the performance of the previously analyzed architecture is evaluated within a TSMC 90nm process. The simulations are conducted on the layout implementation, shown in Fig. 7. It is designed according to the common-centroid technique with additional dummy transistors.

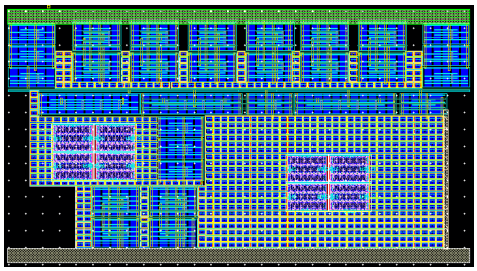

Fig. 7: The layout of the implemented PMU with area 0.142 mm^2.

The implemented PMU is tested at all process (TT, FF, SS, FS, SF), voltage (0.8V, 0.9V, 1V) and temperature (-40°C, 27°C, 125°C) corners. The results for the various performance parameters are summarized in Table IV, where the column entitled 'Typ' corresponds to the nominal corner (TT, $V_{dd} = 0.9$V, 27°C), while the other two columns, 'Min' and 'Max', refer to the lowest and highest value of each index as this is evaluated after the simulations. The load condition for the test is $I_{Load} = 100$ µA ‖ $C_{Load} = 50$ pF.

TABLE IV: Performance Results

Parameter	Min	Typ	Max
Supply voltage (V)	0.8	0.9	1
Regulated output voltage (mV)	599.5	600.3	608.1
Output currents (nA)	7.87	9.03	13.45
Power Consumption (µW)	0.215	0.591	1.7805
PSRR @ DC (dB)	20.92	48.43	87.46
PSRR @ 100kHz (dB)	23.54	25.19	25.78
PSRR @ 1MHz (dB)	23.62	25.3	25.75
Worst PSRR (dB)	20.92	25.15	25.65
Output noise@1Hz (dBV/$\sqrt{Hz}$)	-105.4	-104.5	-103
Output noise@1kHz (dBV/$\sqrt{Hz}$)	-134.4	-130.8	-128.1
Output noise@10kHz (dBV/$\sqrt{Hz}$)	-136.6	-133.1	-131.3
Output noise@100kHz (dBV/$\sqrt{Hz}$)	-151.5	-148.3	-142.6
Output noise@1MHz (dBV/$\sqrt{Hz}$)	-173.3	-170.4	-165.4
DC Gain (dB)	33.83	46.78	79.52
Phase Margin (°)	84.14	87.62	88.79
Unity Gain Frequency (kHz)	7.228	14.37	42.92
Start-up time@Zero Load (µsec)	65.3	78.4	103.7

V. Conclusion

In conclusion, in this paper a process and temperature insensitive Power Management Unit for low-voltage and low-power applications was introduced. It encompasses a BGR, a LDO and a constant g_m circuit, providing stable voltage and current outputs. The design flow utilized Cadence IC Suite with a TSMC 90nm CMOS process. Through post-layout simulations conducted under various conditions valuable insights into the unit's performance were gleaned. The results not only affirm the efficacy of the proposed design but also highlight its robustness accross a range of operating conditions.

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