A General Purpose 2MHz $68\mu W$ Temperature Compensated Reference Clock Oscillator

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***Abstract*—This paper presents a general-purpose 2MHz Reference Clock Oscillator that features temperature compensation in the range of -40$^{\circ}C$ to 70$^{\circ}C$. In other words, through a feedback loop and the use of temperature-stable I_{ref} and V_{ref} sources, it manages to maintain a stable frequency despite temperature variations. It consists of a Current Starved Ring Voltage Controlled Oscillator, a Frequency to Voltage Converter and a Discrete Integrator. The proposed architecture is designed to be area efficient, operating at low power consumption ($68\ \mu W$), and at a low supply voltage (1V). The architecture is simulated using the Cadence IC Suite in a TSMC 90nm CMOS process.**

***Index Terms*—Analog VLSI, Low Power design, Voltage Controlled Oscillator, General Purpose architecture, Temperature Compensation**

I. Introduction

The dependence of a system's performance on the quality of the clock that drives it is significant. Systems used in biomedical, sensor, and system-on-a-chip (SOC) applications demand an exceptionally stable clock, especially in the face of temperature variations [1], [2]. Generally, Crystal Oscillators manage to address this issue but prove unsuitable in many cases due to their inability to be integrated on-chip. This limitation results in increased system size and cost [3]. Therefore, on-chip solutions that provide clock stability need to be developed. One effective approach to achieve this is the design of a system that, through feedback mechanisms, self-regulates to maintain a consistent frequency in changing environmental conditions.

The rest of this work is organized in the following manner. Section II provides an overview of the complete architecture and its function. All subsystems are presented in detail in in Section III. Simulation results and a comparison study are provided in Section IV. Finally, Section V presents some concluding remarks.

II. Oscillator's Architecture

The topology of the implemented architecture is presented in this Section. Initially, the VCO starts oscillating at the free-running frequency, which is significantly higher than the eventual 2MHz target frequency. This frequency is converted into voltage through the Frequency to Voltage Converter and compared to a reference voltage, thereby generating a control signal. This signal is fed back to the VCO, regulating it to oscillate at the predetermined frequency [1]. Fig. 1 depicts the overall architecture, while Fig. 2 illustrates the waveforms of the output and control signal against time.

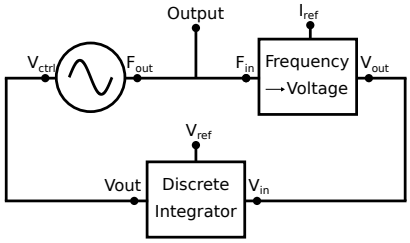

Fig. 1: Architecture Overview

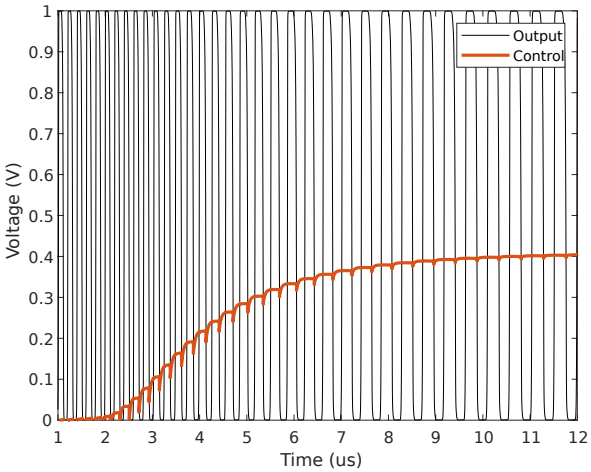

Fig. 2: Output and Control Signal

III. Basic building blocks

A. Voltage Controlled Oscillator

To generate the controlled oscillation, a Current Starved Ring VCO is utilized. In general, a Ring VCO employs an odd number of inverters (n) connected in a circular fashion. Each inverter necessitates a specific duration (t_d) to adjust its output in response to a change in its input. This time

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delay is attributed to the process of charging or discharging the capacitances at the output. As a result, the sequential arrangement of these inverters, coupled with the odd count, means that each inverter perceives at its input the output it had nt_d time units ago, but in an inverted state. This results in oscillation at a frequency of $1/(2nt_d)$.

To control this frequency, a Current Starved VCO adjusts, based on an input signal, the current that charges/discharges the capacitances at the inverters' outputs, thereby altering t_d and consequently the oscillation frequency.

Fig. 3 depicts the charging and discharging of a Current Starved inverter according to a current and the waveforms of the outputs of three inverters, which are connected cyclically to form a Ring VCO.

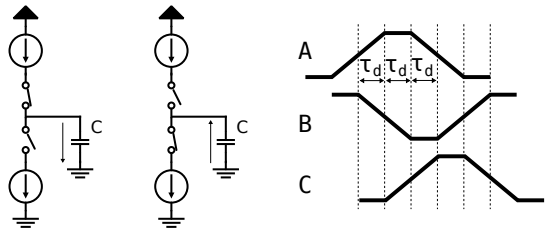

Fig. 3: Current Starved Inverter and 3-Inverter Ring VCO Waveforms

The complete schematic of the Current Starved Ring VCO is depicted in Fig. 4, along with the dimensions of its transistors in Table I. Transistor M_I is responsible for converting the control voltage into a control current. This current is copied through the mirrors consisting of M_n and M_p and ultimately drives the N_1 inverters. The N_2 inverters are used as buffers and are introduced to the outputs of all VCO inverters so that they all see the same capacitance. In the rest of the circuit, N_3 inverters are utilized because they have a higher driving capability and, consequently, can control switches.

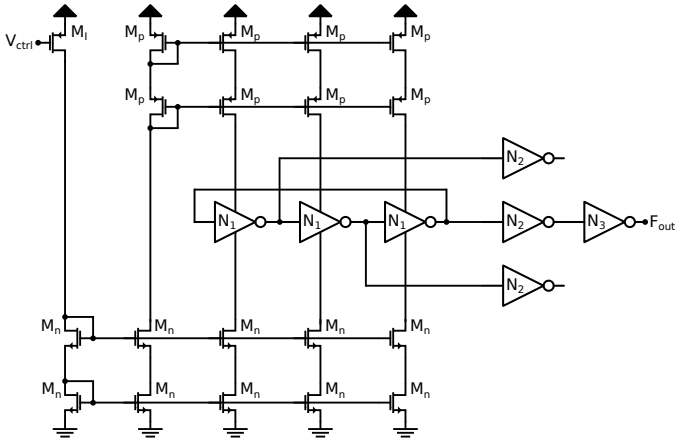

Fig. 4: Schematic of Current Starved Ring VCO

B. Frequency to Voltage Converter

In Fig. 5, the circuit of the Frequency to Voltage Converter [4] is presented, while Table III displays the dimensions of its transistors and Table II those of NOT and NAND gates. This

TABLE I: MOS Transistors' Dimensions (Fig. 4).

NMOS	W/L (μm/μm)	PMOS	W/L (μm/μm)
M_I	0.8/12.4	M_p	1.6/1.6
M_n	0.8/1.6	-	

TABLE II: MOS Transistors' Dimensions (Inverters).

	NMOS	W/L (μm/μm)	PMOS	W/L (μm/μm)
N_1	M_n	0.8/0.48	M_p	6.4/0.48
N_2	M_n	0.8/0.5	M_p	2.4/0.5
N_3	M_n	12.8/0.8	M_p	38.4/0.8
$Nand$	M_n	12.8/0.8	M_p	38.4/0.8

circuit enables the generation of a voltage from the frequency of the VCO, which will provide feedback and readjust the frequency.

This converter operates in three phases. During the first half of the period of the input signal when it is at logic 0, the current I_{ref} charges the capacitor at a rate of I_{ref}/C_1. In the second half of the period, two brief actions take place. First, capacitors C_1 and C_2 are connected to each other, and due to charge redistribution, capacitor C_2 charges. Then, C_2 is isolated, and C_1 fully discharges because it is connected to V_{ss}. This process is summarized in Fig. 6. The two control pulses used in the second half of the period are generated by the "Delay Pulses" circuit. The schematic of this circuit is shown in Fig. 7 and Fig. 8 illustrates the two pulses in relation to the input signal.

If the input frequency is constant and has 50% duty cycle, the output voltage of the circuit is equal to:

$$V_{out} = \frac{I_{ref}}{C_1}\frac{T}{2} = \frac{I_{ref}}{2C_1 f} \tag{1}$$

Additionally, since the pulses used during conversion last for a certain time interval, τ1 and τ2, the maximum frequency that can be converted is:

$$f_{max} = \frac{1}{2(\tau_1 + \tau_2)} \tag{2}$$

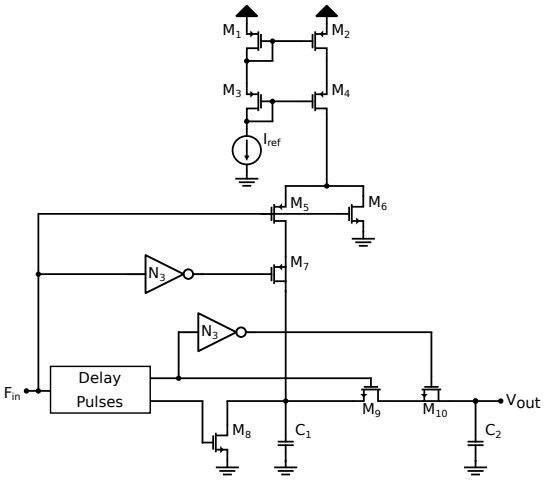

Fig. 5: Schematic of Frequency to Voltage Converter

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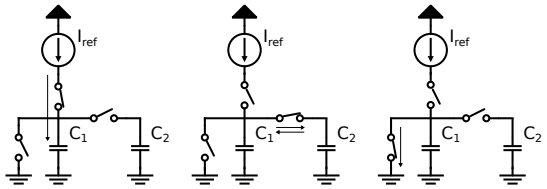

Fig. 6: Operation of Frequency to Voltage Converter

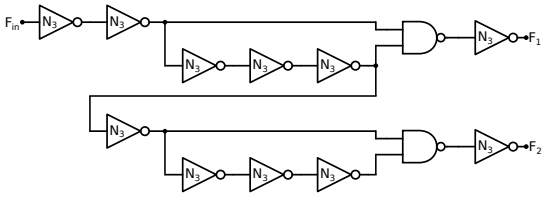

Fig. 7: Schematic of Delay Pulses

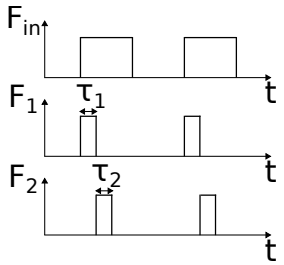

Fig. 8: Waveform of Delay Pulses

TABLE III: MOS Transistors' Dimensions (Fig. 5).

NMOS	W/L (µm/µm)	PMOS	W/L (µm/µm)
M_6	0.8/0.4	M_1-M_4	6.4/1.6
M_8-M_9	11.2/0.4	M_5	1.6/0.4
M_{10}	5.6/0.4	M_7	0.8/0.4

C. Discrete-Time Integrator

To achieve both the frequency to voltage conversion and the comparison with a reference voltage V_{ref}, a Discrete Integrator is employed. This arrangement can replace the part with the capacitors in the Frequency to Voltage Converter, as depicted in Fig. 9. According to the law of conservation of electric charge, it follows that the output of the integrator is equal to:

$$V_{out}[n] = \frac{C_1}{C_2}(V_{ref} - V_{-}) + V_{out}[n-1] \tag{3}$$

Therefore, in the steady state where the voltage generated by the converter at the inverting input of the amplifier equals the reference voltage, the output remains stable. If there is any temperature fluctuation that affects the VCO frequency, this architecture will self-adjust so that the voltage of the converter is once again equal to the temperature-independent source V_{ref}.

Furthermore, the ratios of capacitors C_1 and C_2 represent the step of correction and, therefore, should be chosen carefully. This is because a large step would induce significant variations in the output of the Integrator, which could potentially push the VCO voltage beyond its limits, causing it to shut down. Conversely, if the step is too small, the frequency correction process would be delayed, resulting in periods of irregular frequency.

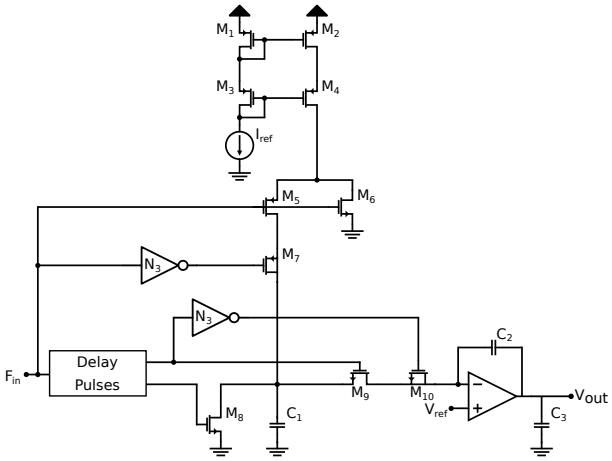

Fig. 9: Schematic of Frequency to Voltage Converter with Integrator

D. Operational Amplifier

The Operational Amplifier that is used is a Folded Cascode with Large-Swing Current Mirrors, which is the ideal choice when the supply voltage is low. Additionally, capacitor C_3 is employed as a compensation capacitor. The bandwidth of the amplifier does not need to be very large as the frequency of the signal it produces at its output is equal to the rate of temperature change, which changes relatively slowly.

The schematic of the amplifier is depicted in Fig. 10, while Table V presents the dimensions of its transistors. In Table VI, the values of the resistors and capacitors used in both the amplifier and the Frequency to Voltage Converter are shown.

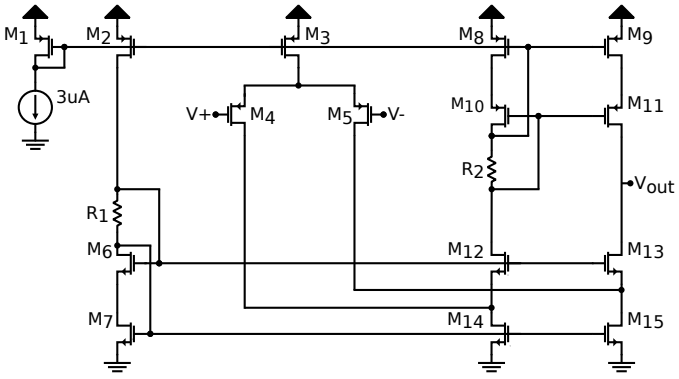

Fig. 10: Schematic of Operational Amplifier

TABLE V: MOS Transistors' Dimensions (Fig. 10).

NMOS	W/L (µm/µm)	PMOS	W/L (µm/µm)
M_6-M_7	3.2/0.8	M_1	6.4/0.8
M_{12}-M_{13}	6.4/0.8	M_2	3.2/0.8
M_{14}-M_{15}	9.6/0.8	M_3	32/0.8
-	-	M_4-M_5	25.6/0.8
-	-	M_8-M_{11}	25.6/0.8

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TABLE IV: Oscillators' Performance Comparison

	Process	Supply	Frequency	Temperature Range	Frequency Variation against Temperature	Power Consumption	Area
This work	TSMC 90nm	1 V	2 MHz	-40°C - 70°C	±1.72%	68 μW	0.13 mm^2
[1]	0.18μm	1.2 V	10 MHz	-20°C - 120°C	±0.4%	80 μW	0.22 mm^2
[2]	65nm	1 V	1.05 MHz	-15°C - 55°C	±0.17%	69 μW	*2.5 mm^2
[3]	0.25μm	2.4 V	7 MHz	-40°C - 125°C	±0.78%	1.5 mW	*1.6 mm^2
[5]	0.18μm	1.2 V	13.4 MHz	-20°C - 100°C	±2%	157.8 μW	0.039 mm^2

Note: *with pads

TABLE VI: Resistors of Operational Amplifier and Capacitors

Capacitors	pF	Resistor	$k\Omega$
C_1	1	R_1	33
C_2	5	R_2	66
C_3	5	-	-

IV. Simulation Results and Comparison

The proposed architecture was simulated using a supply voltage of $1V$ and reference sources $V_{ref} = 0.5V$, $I_{ref} = 2\mu A$, along with appropriate initial conditions. In the beginning, a temperature sweep from $-40°C$ to $70°C$, utilizing the typical transistor models, was conducted. This method was employed to measure the circuit's ability to maintain its frequency concerning temperature variations. The results are presented in Table VII. Subsequently, Monte Carlo simulations were performed with the outcomes depicted in Table VIII. It is crucial to minimize frequency variations due to transistor mismatches. The layout of the implemented clock oscillator is presented in Fig. 11.

TABLE VII: Typical Performance over Temperature Variation

Parameter	Min	Typ	Max
Frequency [MHz]	2.004	2.052	2.065

TABLE VIII: Monte Carlo Performance

Parameter	Mean	Standard Deviation
Frequency	2.062 MHz	41.16 KHz

Finally, corner simulations were executed. Although the frequency experienced some non-negligible changes depending on the process corner, it managed to remain quite stable concerning supply voltage and temperature variations, as shown in Table IX.

TABLE IX: Performance over PVT Variations

Parameter	Mean	Standard Deviation
Frequency	2.074 MHz	155.8 KHz

Table IV illustrates the architecture's performance compared to similar works. The current implementation offers several advantages, such as low power consumption and a wide temperature range, albeit sacrificing some frequency stability. Nevertheless, it represents a highly viable solution for numerous applications.

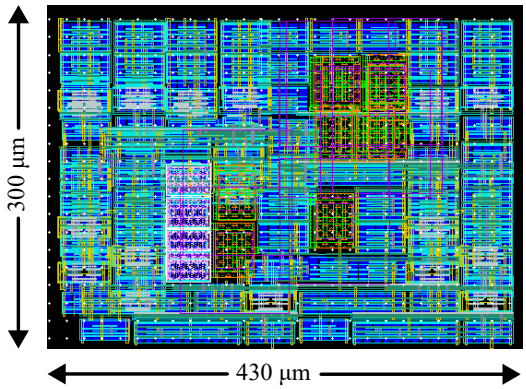

Fig. 11: Layout of the implemented clock reference oscillator in TSMC 90nm

V. Conclusion

In conclusion, in this paper a versatile 2MHz Reference Clock Oscillator, specifically designed to resist temperature variations in the range of -40°C to 70°C, was introduced. It used a feedback loop and the utilization of temperature-stable I_{ref} and V_{ref} sources to ensure the frequency remained stable even under varying thermal conditions. The overall architecture emphasized in efficiency, operating at $68\mu W$ of power consumption and with a low supply voltage of 1V.

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