A 93nW, Analog, Parallel-Connected Threshold Classifier for Epileptic Seizure Prediction

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***Abstract*—This paper introduces an analog front-end classification system designed to function as a wake-up engine for digital back-ends, with a specific focus on predicting epileptic seizures. Accurate seizure prediction is crucial for enhancing the patient's quality of life, as seizures can lead to debilitating consequences and, in severe cases, even fatalities. Existing solutions often rely on power-hungry embedded digital inference engines, consuming considerable amounts of energy, ranging from several μW to mW. To address this limitation and extend the autonomy of embedded devices, we propose a novel approach of a parallel-connected threshold binary classifier, tested on a real-world epileptic seizure dataset. It consists of parallel-connected Gaussian function and Winner-Takes-All circuits. The classifier is designed to be chip-area efficient, operating at minimal power consumption (93 nW), and at a low supply voltage (0.6V), enabling continuous long-term operation. The proposed system is designed and simulated using the Cadence IC Suite in a TSMC 90nm CMOS process, achieving a good specificity of 70%.**

***Index Terms*—Analog VLSI, Ultra-low Power design, Epileptic Seizure Prediction, Wake-up circuit, Threshold Classifier**

I. Introduction

Advancements in wearable technology have led to the emergence of efficient devices suitable for diverse Internet of Things (IoT) applications [1]. Among the areas of interest in the IoT domain, biomedical engineering stands out as a popular research topic [2]. IoT-based wearable sensors offer a cost-effective, reliable, and energy-efficient solution for clinical patient monitoring and disease detection [3]. An illustrative example of such monitoring involves the use of electroencephalogram (EEG), where metal discs (electrodes) are placed on the scalp to measure brain electrical activity [4]. Continuous EEG monitoring can aid in predicting epileptic seizures, identifying sleep disorders, detecting brain damage resulting from head injuries and assessing anesthesia levels during surgery [4].

The utilization of IoT-wearable devices with real-time monitoring and interconnection capabilities enables the efficient collection, sharing and management of patient-related information including diagnosis, therapy, medication, recovery and inventory [5]. By performing the necessary computations closer to the patient (at the edge), these techniques facilitate reduced response times and lower latency, a concept commonly known as edge computing [6]. The reliance on battery-powered and space-efficient devices necessitates the exploration of new computing paradigms [7]. To address the challenges posed by power consumption and high latency, edge computing, when integrated with analog computing [8], emerges as a promising solution. By leveraging physical laws that govern the behavior of transistors, such as analog translinear circuits, mathematical models can be approximated effectively [8]. This, in conjunction with the advantages offered by the sub-threshold region, leads to the development of more power-efficient architectures [9].

Many of the applications mentioned in the context rely on devices that are dependent on battery power and limited in chip area. In light of the increasing demand for area and power-efficient devices, especially with growing computation requirements, we propose an ultra-low power (93nW) analog integrated and area-efficient threshold classifier suitable for epileptic seizure prediction applications [10]. It is a promising wake-up engine appropriate for power-hungry digital back-ends, since it has high sensitivity (100%, accurately predicting all 17 seizures) and good specificity (70%) The post-layout simulation results, conducted in a TSMC 90nm CMOS process and simulated using Cadence IC Suite, validate the accuracy of the implementation by comparing it with a software-based counterpart. Moreover, a comparison study between the proposed classifier (wake-up circuit) and cascaded bell-shaped classifiers is provided.

The remainder of this paper is organized as follows. Section II provides an explanation of the mathematical background related to the proposed analog integrated threshold classifier. In Section III, the main building blocks and the proposed architecture of the classifier are presented. The validation of the proposed classifier is carried out using a real-world epileptic seizure dataset in Section IV. This section also includes a comparison between the hardware and software implementations, along with sensitivity tests. A comparison study and discussion is provided in Section V. Finally, Section VI presents concluding remarks summarizing the findings and implications of this study.

II. Threshold Classifier with Linear combinations of Gaussian functions

Threshold classifiers, which are simplified versions of Support Vector Machines (SVMs), are employed in practice to handle situations where classes are not inherently linearly separable [11]. By utilizing a non-linear transformation function,

denoted as $C()$, these classifiers can convert the data into a higher-dimensional feature space, where the classes become linearly or almost linearly separable. A threshold value, I_{th}, is then tuned to distinguish between the classes effectively. The decision rule of the threshold classifier is as follows:

$$y = \begin{cases} 1 & \text{if } C(X) \geq I_{th} \\ 2 & \text{if } C(X) < I_{th} \end{cases}, \quad (1)$$

where y is the prediction of the classifier and $\boldsymbol{X}$ is a given input vector. The straightforward nature of this architecture makes it highly suitable for hardware implementations, as it effectively reduces chip area without compromising classification accuracy.

In this work, in order to describe each sub-class with one feature ($1-D$ Gaussian function) the mathematical model is described by a summation of univariate Gaussian functions (parallel-connected Gaussian function circuits) and it is approximated by:

$$C(X) = \sum_{k=1}^{K} \{C_i(X)\}. \quad (2)$$

In our implementation, $C_i()$ is chosen to be a univariate Gaussian function, given by:

$$C_i(X) = \frac{1}{\sqrt{2\pi\sigma}} e^{\frac{(X-\mu_i)^2}{\sigma_i^2}}. \quad (3)$$

Here, μ and σ are the mean value and covariance matrices of the Gaussian function. The Gaussian function is preferred over other options because it is straightforward to implement.

III. Proposed Architecture

The topology of the analog threshold classifier along with its basic building blocks is presented in this Section. For this implementation, parallel connected Gaussian function circuits [12] and a Winner-Takes-All (WTA) circuit [13] are necessary. The entire classifier operates with the supply voltage set to $V_{DD} = -V_{SS} = 0.3V$ and all transistors are biased in the sub-threshold region.

Each Gaussian function circuit, shown in Fig. 1, is used to generate an univariate Gaussian function curve. The Bell-shaped circuit is composed of a symmetric current correlator (transistors M_{p1} to M_{p6}) in order to produce symmetric Gaussian curves even for small bias currents. Its electronic tuning capability grants precise control over the non-linear transformation function, offering flexibility and accuracy in its behavior. The transistors' dimensions for one Bump circuit are summarized in Table I.

TABLE I: MOS Transistors' Dimensions (Fig. 1).

NMOS	W/L (µm/µm)	PMOS	W/L (µm/µm)
M_{n1},M_{n4}	1.6/0.4	M_{p1},M_{p2}	1.6/1.6
M_{n2},M_{n3}	0.8/0.4	M_{p3}-M_{p6}	0.4/1.6
M_{n5}-M_{n8}	0.4/1.6	-	-
M_{n9},M_{n10}	1.6/1.6	-	-

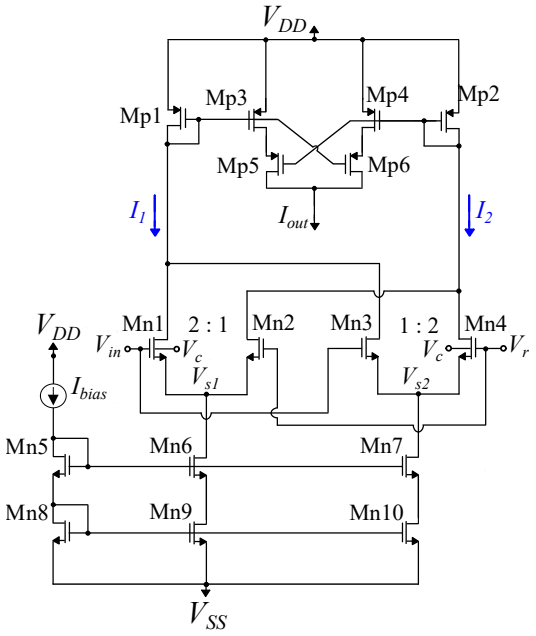

Fig. 1: Univariate Gaussian function circuit. The mean value, variance and height of the Gaussian function are tuned by parameter voltages V_r and V_c, along with the bias current I_{bias}. The voltage V_{in} is the input to the system.

The Winner-Takes-All (WTA) circuit employed in this study functions as an argmax operator, indicating the largest of its inputs. Fig. 2 illustrates a 2-input WTA circuit, in which a constant current is fed as a bias to its second input. As a result, it effectively operates as a current-mode comparator. In the context of our application, this WTA circuit plays a significant role since it is responsible for extracting the classifier's prediction. All transistors' dimensions are set to $W/L = 0.4\mu m/1.6\mu m$.

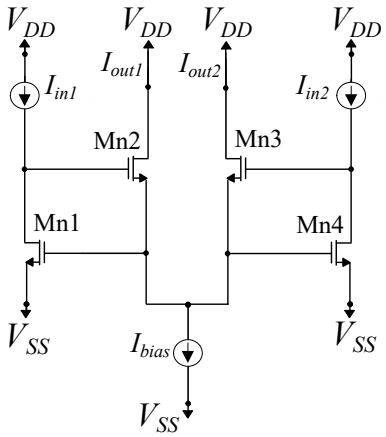

Fig. 2: An 2-neuron Standard Lazzaro NMOS WTA circuit.

The proposed threshold classifier architecture is presented in Fig. 3. It is initially designed to handle a 2-class and 4-feature classification problem. However, it possesses scalability in terms of accommodating input features. In this case only the

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probability of one class is calculated. The resulting current representing this probability is then compared to a fixed threshold current using the WTA circuit. It is important to note that the value of this threshold current has a direct impact on the classifier's specificity (detecting true-positive).

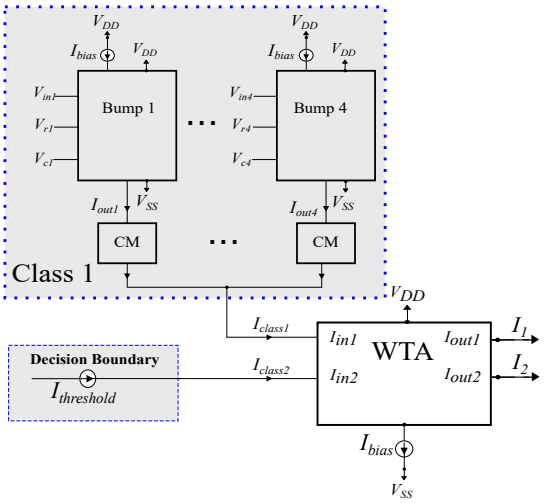

Fig. 3: The proposed classifier's top-level architecture

The proposed implementation utilizes a sum of 4 univariate parallel-connected Gaussian function circuits for the non-linear transformation. The output current of each one of these circuits represents the probability of the input vector to belong to the class according to the corresponding feature. Then, the calculated probabilities of one class are summed through current mirrors (CMs) and the result is finally compared to the threshold current denoted as $I_{threshold}$. The classifier's prediction is described by the output current I_1 of the WTA circuit. The current I_1 is in binary representation, where a logical 1 (high current value) indicates that the first class is the winner, whereas a logical 0 (low current value) signifies the second class as the winner.

IV. Epileptic Seizure Prediction Application and Simulation Results

To test the threshold classifier, a real-world epilepsy seizure prediction problem is applied [10]. The data used in this study are obtained from the CHB-MIT Scalp EEG database [10] and it comprises EEG signals recorded from children with intractable epilepsy. Expert physicians have provided labels for the ictal periods which correspond to the periods of seizures. For this analysis, pre-ictal and post-ictal periods are defined as one hour before and one hour after the seizure, respectively. Data samples that do not fall within the ictal, pre-ictal, or post-ictal periods are labeled as inter-ictal. A high sensitivity score is crucial for the patient's health, as it ensures that all upcoming seizures will be predicted accurately. Also, another metric is specificity, which is the ratio of the time that the digital back-end is idle to the duration of all the inter-ictal periods (no risk for seizure).

To test the proposed classifier both in terms of classification specificity and circuit's behavior over PVT variations, two separate tests are conducted on the layout presented in Fig.4. To address the experimental variability, the results from 20 different training-test iterations are presented in Fig. 5. The sensitivity of the circuit is further validated through a Monte Carlo analysis. More specifically, Fig. 6 illustrates the Monte Carlo Histogram for N = 100 points. The outcomes from both tests are summarized in Table II, providing a comprehensive overview of the circuit's performance and robustness.

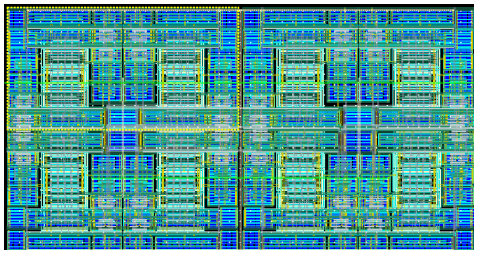

Fig. 4: The layout of the implemented wake-up circuitry

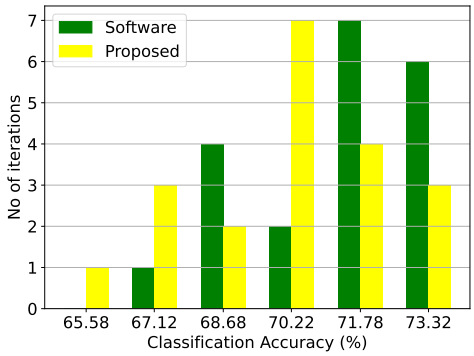

Fig. 5: Classification results of the proposed architecture and the equivalent software model on the dataset over 20 iterations.

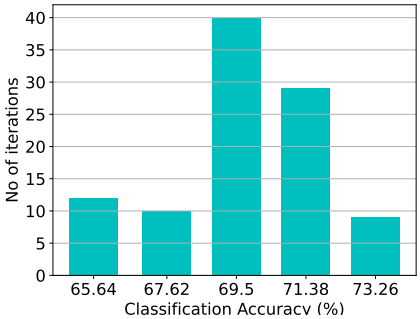

Fig. 6: Post-layout Monte-Carlo simulation results of the proposed architecture on the dataset.

TABLE II: Performance Results

Method	Best	Worst	Mean	Std.
Software	0.741	0.675	0.713	0.019
Proposed	0.732	0.648	0.7	0.021
Monte Carlo	0.742	0.648	0.698	0.022

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TABLE III: Analog classifiers' comparison on the Epileptic Seizure Prediction

	Classifier	Min accuracy	Mean accuracy	Max accuracy	Power consumption	Processing speed	Energy per classification	Estimated area
This work	Threshold	0.648	0.7	0.732	$93nW$	$320K\frac{\text{classifications}}{\text{s}}$	$\frac{0{,}291\text{ pJ}}{\text{classification}}$	$0.009mm^2$
[12]	GMM	0.672	0.691	0.714	$180nW$	$100K\frac{\text{classifications}}{\text{s}}$	$\frac{1.8\text{ pJ}}{\text{classification}}$	$0.026mm^2$
[14]	Fuzzy	0.701	0.723	0.756	$147nW$	$4.55K\frac{\text{classifications}}{\text{s}}$	$\frac{32{,}3\text{ pJ}}{\text{classification}}$	$0.073mm^2$
[15]	Bayes	0.593	0.653	0.688	$123nW$	$100K\frac{\text{classifications}}{\text{s}}$	$\frac{1.23\text{ pJ}}{\text{classification}}$	$0.014mm^2$
[16]	Threshold	0.612	0.667	0.691	$111nW$	$100K\frac{\text{classifications}}{\text{s}}$	$\frac{1.11\text{ pJ}}{\text{classification}}$	$0.010mm^2$
[17]	SVM	0.688	0.703	0.742	$3.24\mu W$	$140K\frac{\text{classifications}}{\text{s}}$	$\frac{23{,}14\text{ pJ}}{\text{classification}}$	$0.11mm^2$
[18]	Centroid	0.632	0.656	0.695	$355nW$	$100K\frac{\text{classifications}}{\text{s}}$	$\frac{3.55\text{ pJ}}{\text{classification}}$	$0.019mm^2$

V. Analog classifiers Summary and Discussion

This section aims to present a comparative analysis of various analog classifiers developed by our research team. By adjusting these classifiers to the same application as the one tested in this work a fair and unbiased comparison can be conducted. In Table III a performance summary is illustrated for a fuzzy [14], a Gaussian Mixture Model (GMM) [12], a Bayesian [15], a cascaded-connected Threshold [16], a Support Vector Machine (SVM) [17] and a centroid-based [18] classifier.

In contrast to the fuzzy [14] and SVM [17] classifiers, the proposed architecture achieves a nearly identical mean classification accuracy while consuming approximately 100 times less energy per classification making it a significantly more energy-efficient choice. Moreover, it outperforms the other analog classifiers in terms of mean accuracy and power- and area-efficiency. It is important to emphasize that, for this specific application, high classification accuracy (specificity) is not a primary requirement because this circuit is used as a wake-up engine for a digital back-end. The necessary characteristic is sensitivity in seizure prediction (successively detects all 17 epileptic seizures) where all classifiers achieve 100%.

VI. Conclusion

An analog integrated, ultra-low power (93nW), parallel-connected threshold classifier was proposed in this work. Its main building blocks are Bell-shaped circuits along with an argmax circuit. A real-world epileptic seizure prediction dataset was used to validate the classifier's specificity. All post-layout simulation results were obtained using the TSMC 90nm CMOS process and were compared with a software-based implementation and a variety of analog classifiers. The proposed wake-up circuit demonstrates a remarkable sensitivity of 100%, accurately predicting all 17 seizures in the test set. Finally, it achieves a specificity of 70%.

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