A 1.8V CMOS Chopper Four-Quadrant Analog Multiplier

Dimitrios Baxevanakis
Department of Electrical and Computer Engineering
National Technical University of Athens
Greece
dimbaxev@central.ntua.gr

Paul P. Sotiriadis
Department of Electrical and Computer Engineering
National Technical University of Athens
Greece
pps@ieee.org

***Abstract*—A 1.8 V CMOS chopper four-quadrant analog multiplier, intending to serve as an autonomous IC block for low-frequency signal processing, is presented. Particular emphasis is laid upon achieving low output noise by means of chopper stabilization, while the multiplier's operation is based on the MOS Translinear Principle. The proposed design has been implemented and simulated in TSMC 0.18 µm CMOS process.**

I. Introduction

Analog multipliers are amongst the most important IC building blocks in both analog and mixed-signal integrated systems. They can be found in a plethora of more complex circuitry, including modulators, RMS-DC converters, phase comparators, phase-locked loops, adaptive filters, frequency synthesizers, neural networks, fuzzy-logic integrated systems, analog computers and more.

In many applications, electronic systems operate in low-frequency ranges where signal processing can be challenging since CMOS integrated circuits may suffer from severe levels of DC-offset and low-frequency (mainly $1/f$) noise. A fine example of such an application field is biomedical signals acquisition and processing; here, typical signal amplitude values are $10\,\mu\mathrm{V}$–$10\,\mathrm{mV}$ in the frequency range of DC–$10\,\mathrm{kHz}$, where offset and $1/f$ noise dominate [1]. In order to overcome these obstacles, the presented multiplier employs chopper stabilization, making it suitable for operation in applications with requirements similar to the above.

Typically, there are two types of CMOS analog multipliers: those operating in sub-threshold region and being based on a Gilbert-Cell type core, and those operating in strong-inversion region using the MOS square-law Translinear Principle. The proposed one is of the second kind, with its non-linear core operating in current-mode and indirectly giving the product of the x- and y-input currents that it is fed with. The complete architecture of the proposed multiplier as a system is depicted in the block-diagram of Fig. 1.

The remainder of this paper is organized as follows. Section II presents the chopper stabilization technique in analog multipliers, while Section III deals with the multiplier's translinear core. The rest of the architecture chain is demonstrated in Section IV, with the simulation results following in Section V. Finally, conclusions and future work are reported in Section VI.

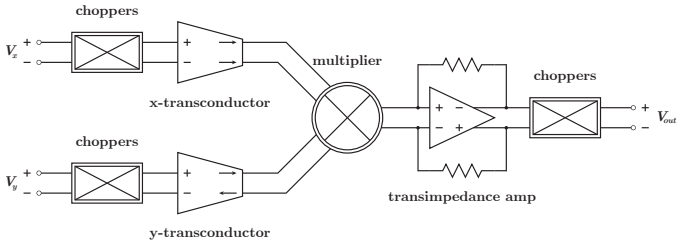

Fig. 1: Architecture of the proposed chopper four-quadrant analog multiplier.

II. Chopper Stabilization in Analog Multipliers

The chopper stabilization technique (or chopping) has long been successfully applied to amplifiers in order to suppress DC-offset and low-frequency noise [2]. The technique can be also applied to analog multipliers, with the general principle of operation given in Fig. 2 [3].

The idea is to modulate and frequency-shift both input signals, V_x and V_y, to a higher frequency band where the noise power spectral density (PSD) is significantly lower than that in low-frequencies, and perform the analog processing in this frequency range. Then, the output product is frequency-shifted back to the baseband. Offset and low-frequency noise of the complete system are modulated only at the output, thus frequency-shifted away from the baseband. A low-pass filter (LPF) can then isolate the desired signal from the unwanted modulation artifacts, giving us ideally an offset- and $1/f$ noise-free result.

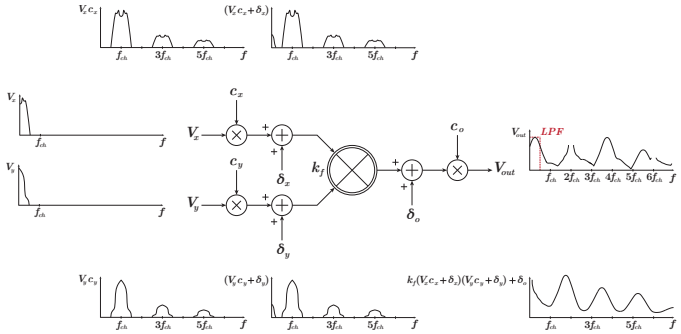

Fig. 2: Chopper stabilization technique in analog multipliers.

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If we choose two quadrature in phase square-waves with a frequency of f_{ch}, levels of ± 1 and 50% duty cycle as our input chopping waveforms, c_x and c_y, and their product as the output chopping waveform, c_o (Fig. 3) [3], the following equations hold:

$$\begin{aligned} c_x c_x = c_y c_y = c_o c_o = 1 \\ c_x c_o = c_y \\ c_y c_o = c_x \end{aligned} \quad (1)$$

From Fig. 2 and assuming a multiplication gain of k_f, equation (1) implies that the output of the chopper multiplier is:

$$V_{out} = k_f V_x V_y + k_f V_x \delta_y c_y + k_f V_y \delta_x c_x + k_f \delta_x \delta_y c_o + \delta_o c_o \quad (2)$$

We observe that all three offset and noise components in the model of a multiplier, δ_x, δ_y and δ_o [4] are frequency-shifted away from the baseband by one of the chopping waveforms, while the desired term $k_f V_x V_y$ remains intact. Note that the input chopping frequency, f_{ch}, must be at least twice the highest frequency component of the input signals (so no aliasing occurs) and the $2f_{ch}$ frequency resulting from multiplication should be low enough for the complete circuit's bandwidth [2], [3].

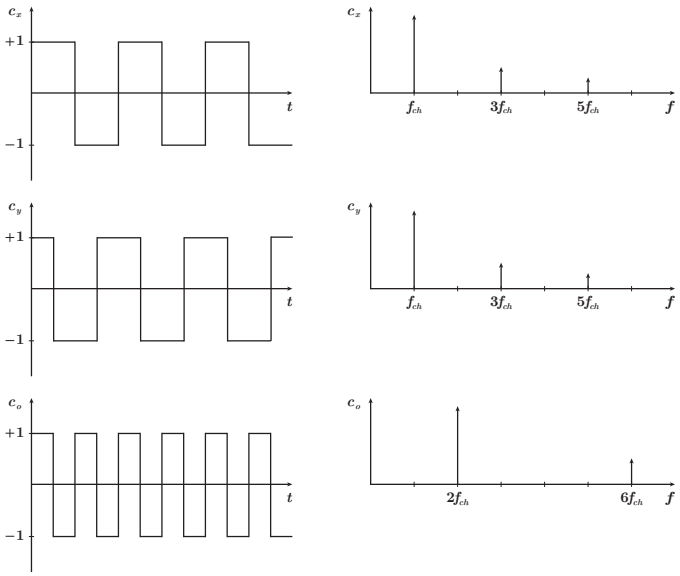


Fig. 3: Chopping waveforms and corresponding spectra.

Choosing square-waves that switch between ± 1 as chopping waveforms makes the implementation of the chopper modulators straightforward in CMOS processes, since we simply need to switch the polarity of the differential input signals. The chopper modulators used in the proposed design are shown in Fig. 4. They consist of two paths enabled by the corresponding transmission gates. Each transmission gate is placed between two half-sized dummy ones to reduce channel charge-injection [2], [5]. The usage of transmission gates instead of simple MOS switches not only helps with the minimization of other non-idealities such as clock-feedthrough [5], but also improves the linearity of the switch over a wider

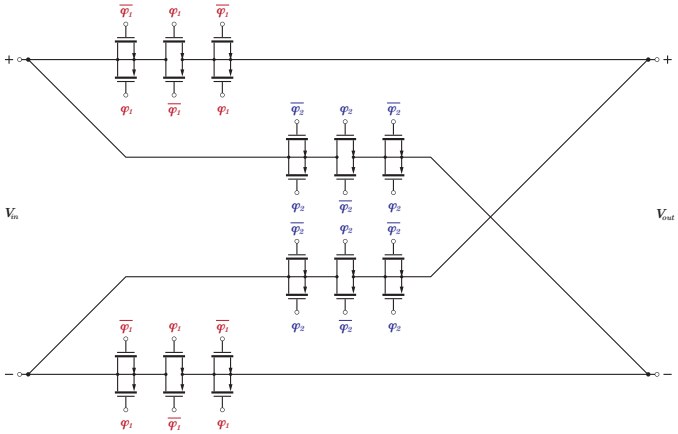


Fig. 4: CMOS chopper modulators.

voltage range. All MOSFETs are minimum-sized to minimize the stray capacitances.

Phases ϕ_1 and ϕ_2 control the path selection, and therefore the input signal polarity, performing the chopper modulation. In order to ensure flawless operation, ϕ_1 and ϕ_2 must be non-overlapping, which can be guaranteed if a non-overlapping clock generator is used for their implementation [5].

III. MOS Translinear Core

The term translinear refers to circuit structures having transconductance linear with respect to an electrical variable. In the case of MOSFETs operating in strong-inversion, the transconductance is proportional to voltage, and the resulting circuit family is known as MOS translinear (MTL) [6].

A. The MOS Translinear Principle

If we consider a loop of NMOS devices, some of them connected in clockwise (cw) fashion and the others counter-clockwise (ccw), by applying Kirchhoff's Voltage Law we straightforwardly get:

$$\sum_{cw} V_{gs} = \sum_{ccw} V_{gs} \quad (3)$$

Assuming that all transistors are in strong-inversion region, as well as equal μ_n, C_{ox} and V_{th} values, equation (3) transforms into:

$$\sum_{cw} \sqrt{\frac{I_{ds}}{\frac{W}{L}}} = \sum_{ccw} \sqrt{\frac{I_{ds}}{\frac{W}{L}}} \quad (4)$$

Same results are obtained if we use PMOS devices in the loop. By manipulating the number of transistors in the translinear loop, their $^{W}/_{L}$ values and drain currents, we are able to implement a vast number of mathematical expressions in the form of current [6].

B. Translinear Four-Quadrant Multiplier Core

Fig. 5 presents the proposed translinear multiplier core. It consists of two translinear loops, M_1–M_4 and M_3–M_6, each one being a current-squaring circuit. Transistors $M_{1'}$ and $M_{5'}$ enable us to get $I_1 + I_2$ and $I_5 + I_6$ as intermediate

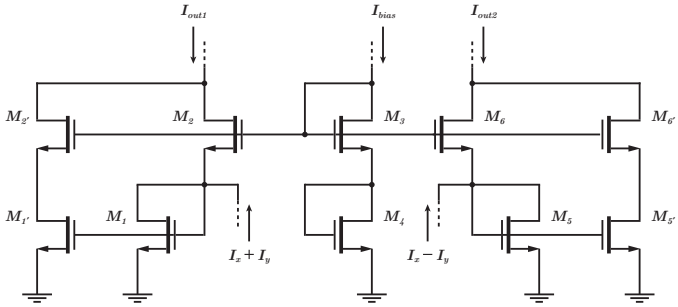


Fig. 5: Translinear multiplier core.

outputs, while cascodes $M_{2'}$ and $M_{6'}$ are added to improve the V_{ds}-matching of M_1–$M_{1'}$ and M_5–$M_{5'}$, resulting in better mirroring of their currents. All MOSFETs feature the same $^W/_L$ values.

Driving the circuit with $I_x + I_y$ and $I_x - I_y$ input currents as denoted and applying the MOS Translinear Principle, it can be shown that:

$$\begin{aligned} I_{out_1} &= 2I_{bias} + \frac{(I_x + I_y)^2}{8I_{bias}} \\ I_{out_2} &= 2I_{bias} + \frac{(I_x - I_y)^2}{8I_{bias}} \end{aligned} \tag{5}$$

So, taking $I_{out_1} - I_{out_2}$ as the differential current output of the structure, I_{out}, we acquire the desired multiplication of I_x and I_y quantities:

$$I_{out} = \frac{(I_x + I_y)^2}{8I_{bias}} - \frac{(I_x - I_y)^2}{8I_{bias}} = \frac{I_x I_y}{2I_{bias}} \tag{6}$$

IV. Complete System Architecture

The complete system architecture of the proposed chopper four-quadrant analog multiplier is shown in Fig. 1. It is composed of the input and output choppers, whose basic block was presented in Section II, the translinear multiplication core discussed in the previous section and the essential V–I and I–V converters needed for the current-mode operation of the core.

A. X- and Y- Input Transconductors

The V–I conversion at the system's inputs is achieved via two transconductors, the x-input one depicted in Fig. 6 [7].

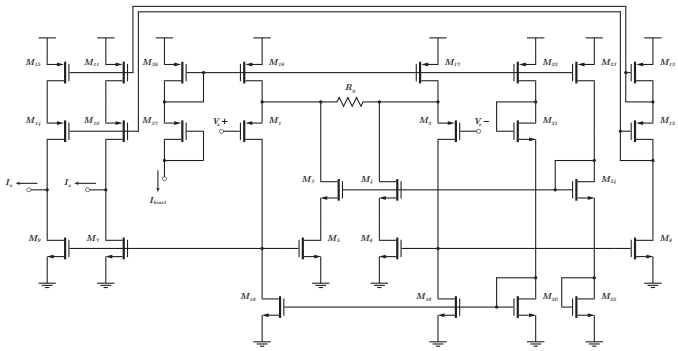
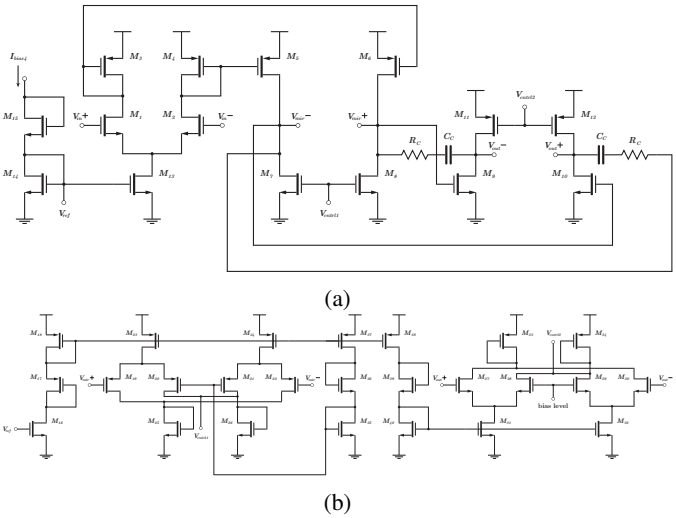


Fig. 6: X-input transconductor.

A passive resistor is preferred over a MOSFET operating in triode region for better linearity. The y-input transconductor shares the same design, the only difference being a modified current-mirroring circuitry; y-input transconductor must simultaneously feed and draw the I_y current needed for implementing the translinear core inputs $I_x + I_y$ and $I_x - I_y$, as opposed to x-input transconductor that simply feeds the I_x current twice.

B. Transimpedance Amplifier

The I–V converter in our design is a fully-differential transimpedance amplifier, consisting of a miller-compensated fully-differential current-mirror operational amplifier [7] with a common-source output stage. The amplifier has its inputs tied to the corresponding output nodes through passive resistors (Fig. 1), the value of which can be altered based on the desired output voltage swing. Due to its fully-differential structure, a common-mode feedback (CMFB) network to determine and control the amplifier's common-mode voltages is mandatory [7]. The operational amplifier and its continuous-time CMFB network are shown in Fig. 7.



(a)

(b)

Fig. 7: Fully-differential operational amplifier (a) and CMFB network (b) used in the transimpedance amplifier.

V. Simulation Results

The proposed multiplier has been designed in TSMC $0.18\,\mu\text{m}$ CMOS process, with a single $1.8\,\text{V}$ power supply. Cadence® Spectre® simulations give a total power consumption of $1.51\,\text{mW}$ for the complete system, including all additional circuitry not presented here (non-overlapping clock generators, biasing circuitry). The DC transfer characteristics of the multiplier with an input voltage range of $\pm 50\,\text{mV}$ that can be seen in Fig. 8 demonstrate good linearity performance. Maximum offset in the aforementioned range is $5\,\mu\text{V}$, rising about $1\,\mu\text{V}$ per $10\,\text{mV}$ absolute rise in y-input.

For the chopping operation, we set $f_{ch} = 100\,\text{kHz}$, a frequency high enough for various applications, and drive the multiplier with two sinusoid inputs of $10\,\text{kHz}$ (x-input)

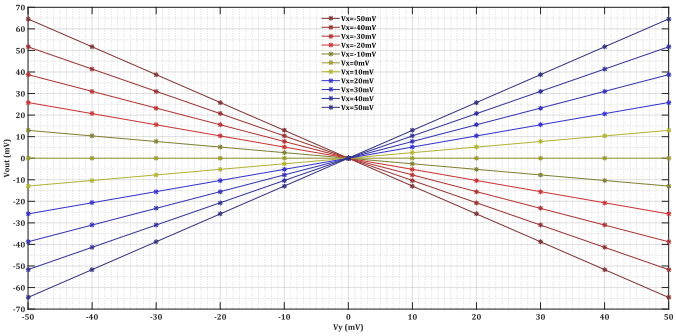


Fig. 8: Multiplier's DC transfer characteristics with V_x and V_y ranging from $-50\,\mathrm{mV}$ to $50\,\mathrm{mV}$.

and $11\,\mathrm{kHz}$ (y-input), each with an amplitude of $50\,\mathrm{mV}$. The choice of such close input frequencies is made to minimize the spectral interference of modulation artifacts to the desired output product (expecting peaks at $1\,\mathrm{kHz}$ and $21\,\mathrm{kHz}$). The output spectrum is shown in Fig. 9. The desired signal components of the multiplication at frequencies $1\,\mathrm{kHz}$ and $21\,\mathrm{kHz}$ are the strongest ones at $-29.8\,\mathrm{dB}$ while the next one in the $0\,\mathrm{Hz}$–$50\,\mathrm{kHz}$ range lies at $-99.5\,\mathrm{dB}$, implying a spurs-free dynamic range (SFDR) of $69.7\,\mathrm{dB}$. Fig. 10 (a) gives the transient output of the same simulation, with a simple 1st-order differential LPF ($R_{LPF} = 270\,\mathrm{k\Omega}$, $C_{LPF} = 20\,\mathrm{pF}$ giving a cut-off at $29.47\,\mathrm{kHz}$) added at the end of the system chain; Fig. 10 (b) demonstrates the ideal x·y product.

Finally, Fig. 11 illustrates the multiplier's output noise PSD. The low-frequency noise alongside with DC-offset have been moved upward in frequency, placed at $2f_{ch}$ and its odd harmonics, as predicted.

VI. Conclusions

A CMOS four-quadrant analog multiplier is presented, using chopper stabilization to suppress DC-offset and low-frequency noise, thus making it a capable signal processing IC block for low-frequency applications. Its core consists of a MOS translinear circuit that implements non-linear multiplication in current-mode, while the system's simulated overall performance is in line with theory, giving promising results for a real-life implementation. Future goals of the authors include the derivation of an analytic non-linear model for the complete system, as well as making improvements on various aspects of the proposed design that would lead to fabrication of the IC and bench measurements.

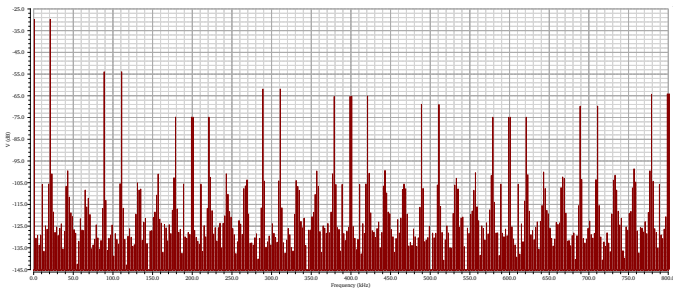
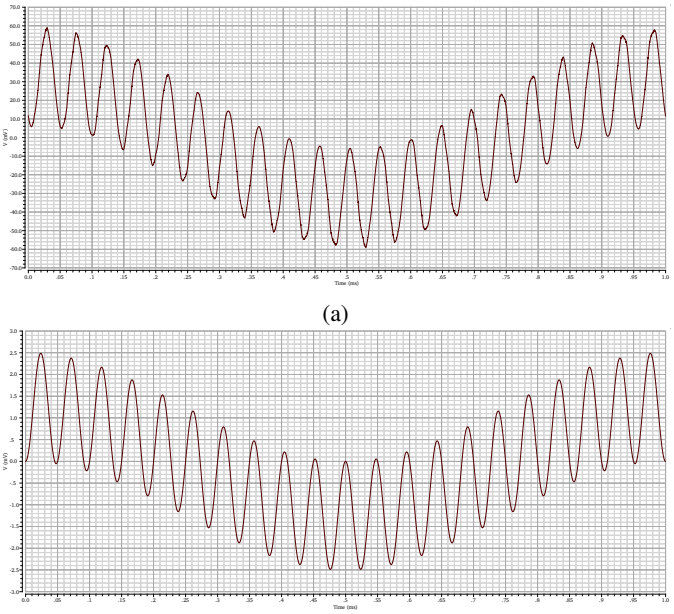


Fig. 9: Output spectrum for sinusoid inputs of $10\,\mathrm{kHz}$ and $11\,\mathrm{kHz}$ with a $50\,\mathrm{mV}$ amplitude.



(a)

(b)

Fig. 10: Transient output for the same inputs after a 1st-order differential LPF (a) and ideal multiplication product (b).

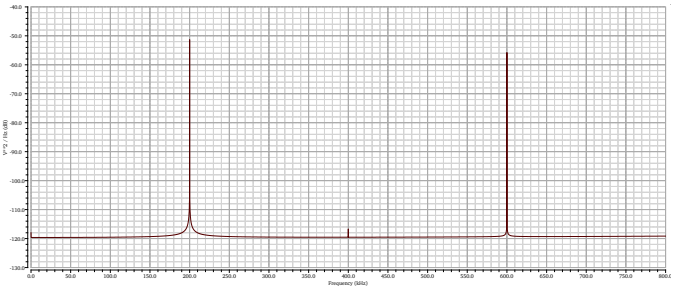


Fig. 11: Multiplier's output noise PSD.

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