A 0.6V, 700nW Chopper Capacitively-Coupled Instrumentation Amplifier for Biomedical Applications

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***Abstract*—This work presents the analysis and design of a CMOS capacitively-coupled instrumetation amplifier (CCIA). The amplifier has a gain of 40 dB for frequencies up to 100 Hz with ultra-low power consumption, thus being suitable for portable health monitoring devices. The reduction of power consmuption is achieved by biasing the MOSFETs of the circuit in the subthreshold region. Chopper stabilization is employed to eliminate the dominant low-frequency noise. The CCIA is implemented by means of Cadence® Custom IC Design Tool in TSMC 0.18 µm process.**

***Index Terms*—bio-signal amplification, ultra-low power, subthreshold, chopper stabilization, $1/f$ noise**

I. Introduction

Monitoring patients' health daily in their everyday environment is in many cases necessary to prevent crises that can put their lives in danger (such as epilepsy, heart attacks, etc). There is, thus, the need for designing portable devices which amplify and process biopotential signals. Such devices should have minimum size and ultra-low power consumption in order to enhance portability. Biopotential signals are low-amplitude, low-frequency signals, conditions that require an accordingly low system noise. Generally, the front-end of biopotential acquisition systems consists of three parts: a low-power instrumentation amplifier (IA), a switched-capacitor filter and an analog-to-digital converter (ADC), as shown in Fig. 1.

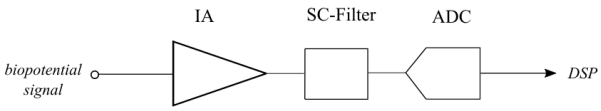

Fig. 1. Front-end for the processing of biopotential signlas.

This paper presents the design of an amplification front-end stage, which is implemented as a CMOS capacitively-coupled instrumentation amplifier with a gain of 40 dB. The design focuses on EEG signals, which have amplitudes that vary between 1 µV and 100 µV, for frequencies up to 100 Hz. In order to achieve low power consumption, MOSFETs are biased in the subthresold region. Furthermore, the chopper stabilization technique (CHS) is used to deal with the low-frequency noise.

The remainder of the paper is organized as follows. Section II briefly describes the MOSFET operation in the subthreshold region and Section III presents the principles of chopper stabilization. The architecture of the proposed circuit is shown in Section IV, followed by the simulation results in Section V. The paper ends with conclusions drawn in Section VI.

II. MOSFET Subthreshold Operation

A. DC Operation

In the subthreshold region (or weak inversion) the drain current of a MOSFET is given by [1]:

$$I_D = I_{spec}\left(e^{\frac{V_G - V_t}{nU_T}}\right)\left(1 - e^{-\frac{V_{DS}}{U_T}}\right) \tag{1}$$

where

$$I_{spec} = 2n\mu C_{ox}\frac{W}{L}U_T^2 \tag{2}$$

U_T is the thermal voltage. The current is saturated for $V_{DS} > 4U_T$. For values of n near 1, we get:

$$I_{D,sat} = I_{spec}\left(e^{\frac{V_{GS} - V_t}{nU_T}}\right) \tag{3}$$

The transconductance is given by [1]:

$$g_m \triangleq \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nU_T} \tag{4}$$

B. Noise

In weak inversion MOSFETs suffer from shot noise and flicker noise (or $1/f$ noise) [2]. Shot noise is white noise with a PSD given by [3]:

$$\overline{i_{sn}^2}(f) = 2qI_D \tag{5}$$

Flicker noise is frequency-dependent and its PSD is given by [1]:

$$\overline{i_{fn}^2}(f) = \frac{4kT\rho}{WL}\frac{g_m^2}{f} \tag{6}$$

ρ is a process-dependent constant ($\rho \propto C_{ox}^{-\alpha}, 1 < \alpha < 2$).

When the current is saturated ($I_D = I_{D,sat}$) the total noise PSD equals:

$$\overline{i_n^2}(f) = 2qI_{D,sat} + \frac{4kT\rho}{WL}\cdot\frac{g_m^2}{f} \tag{7}$$

The PSD of the total noise is depicted in Fig. 2

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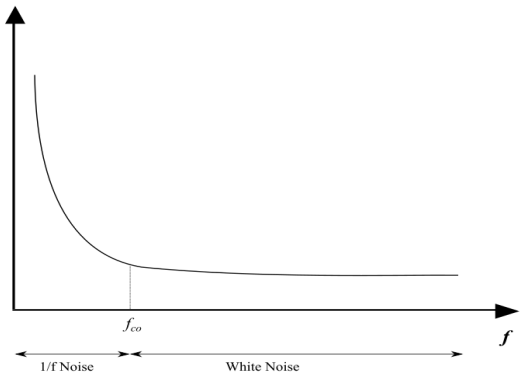

Fig. 2. Total noise PSD.

III. Chopper Stabilization

The chopper stabilization (CHS) technique is an efficient way to suppress low-frequency noise. As a result, CHS is widely used by analog designers. The general principle is shown in Fig 3.

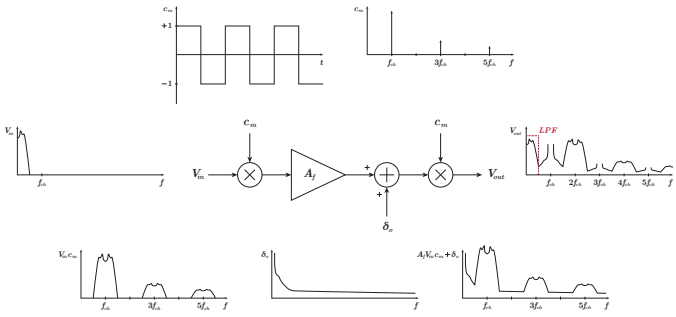

Fig. 3. General principle of the CHS technique.

The idea is to modulate the signal to a higher frequency where flicker noise is negligible and then demodulate it back to the baseband, after the amplification [4]. The noise added by the amplifier is modulated only once, so the output noise is shifted away from the signal. Using a low-pass filter (LPF) at the output, we can recover the amplified signal. The modulation is performed by multiplying the signal with square-waves $c_m\,(t)$ of period $T = 1/f_{chop}$, levels of ± 1 and duty cycle 50%. By doing so, the output signal is demodulated to the original band, while the noise is transposed to the odd harmonics of $c_m\,(t)$ [4].

It should be noted that f_{chop} must be at least twice the higher signal frequency, in order to avoid aliasing. At the same time, $2f_{chop}$ must be less than the amplifier's bandwidth, so that the upmodulated signal can be properly processed.

Each chopper modulator can be easily implemented, since all we need is the polarity of the differential input to be inverted once in every period. This is achieved by two pairs of switches controlled by complementary clocks. The switches are realized as transmission gates equipped with two half-sized dummy devices, in order to minimize charge injection. The design of the proposed modulator is shown in Fig. 4 [5].

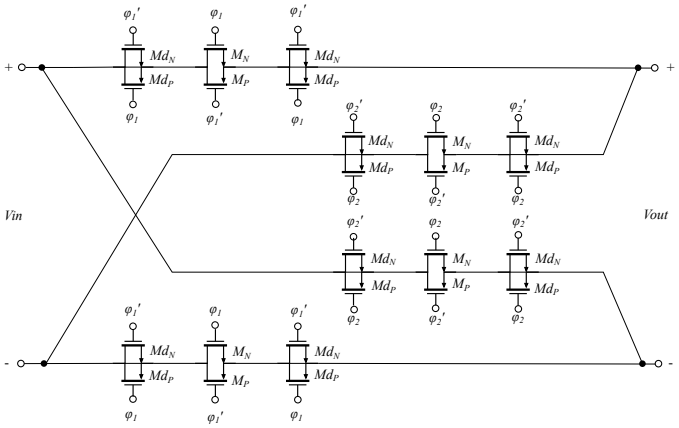

Fig. 4. Chopper modulator.

IV. Architecture of the CCIA

Apart from noise and power consumption, there exist other challenges linked with the interface between the required electrode for the signal's acquisition and the human skin [6]. An electrode offset voltage (EOV) is introduced due to chemical reaction between the metal of the electrode and the electrolyte gel that is used. Its value is large (between $10\,\mathrm{mV}$ and $100\,\mathrm{mV}$) compared to the input signal's amplitude, which means that the input signal needs to be filtered before the amplification. The contact exhibits an equivalent impedance of the order of $2\,\mathrm{M\Omega}$ [7], so the input impedance of the IA must be much greater than that value [6].

A. Overall Architecture

The overall architecture of the proposed circuit is shown in Fig. 5. It consists of an operational transconductance amplifier (OTA), the chopper modulators, input capacitors C_{in}, feedback capacitors C_f, output capacitor C_{out} and bias resistors R_b.

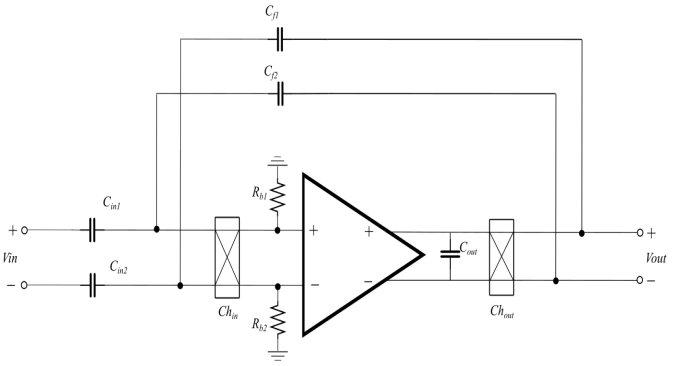

Fig. 5. Proposed CCIA.

The closed-loop gain is approximated by the ratio between the input and the feedback capacitors. By choosing $C_{in1,2} = 50\,\mathrm{pF}$ and $C_f = 300\,\mathrm{fF}$, we achieve a closed-loop gain greater than $40\,\mathrm{dB}$.

An important choice is whether to perform the first modulation before or after the input capacitors. If we place the

first chopper directly at the input, EOV is upmodulated and amplified, saturating the OTA. In such a case a DC-Servo Loop (as in [8], [9]) can be employed. In the proposed design, chopping is performed after the input capacitors, and EOV is passively filtered.

The combination of a chopper modulator with two capacitors is equivalent to a single paracitic resistance $R_{mod} = 1/(2f_{chop}C)$ [6]. If the input modulator is placed in the virtual ground of the amplifier, it sees the parasitic capacitances of the input MOSFETs. These are much smaller than $C_{in1,2}$. As a result, the circuit's input resistance is much greater. Consequently, by placing Ch_{in} before $C_{in1,2}$ we further reduce the circuit's size, while avoiding the danger of instability caused by many loops.

One advantage of an OTA is the ability to set the dominant pole's frequency, which is mainly determined by the product $R_{out}C_{out}$, because of the magnitude of R_{out}. In our design, C_{out} is set to 300 fF.

B. OTA

The OTA is realized as a recycling folded cascode (RFC), as shown in Fig. 6 [10]. The MOSFETs composing the circuit are biased in the subthreshold region.

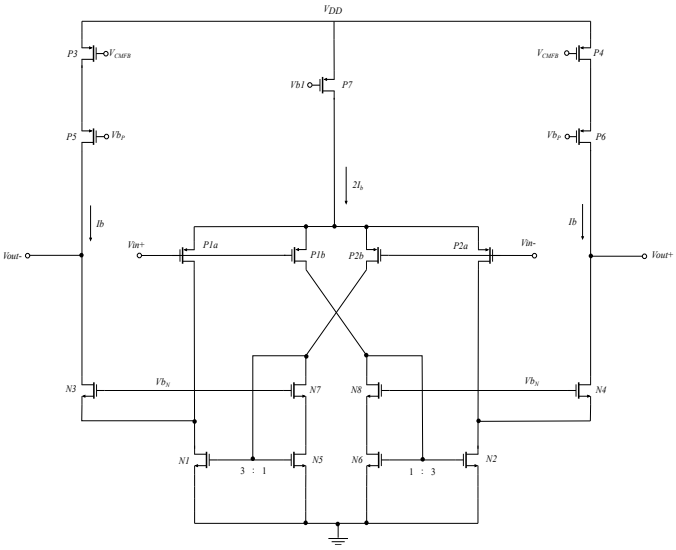

Fig. 6. OTA topology: Recycling Folded Cascode.

With the chosen mirror ratios it can be shown that [10]:

$$G_m = 4g_m \tag{8}$$

where g_m is the transconductance of the input transistors. The open-loop gain is given by:

$$A_V = G_m R_{out} \tag{9}$$

where [10]

$$R_{out} = [g_{m_{N4}} r_{ds_{N4}} (r_{ds_{P2a}} \parallel r_{ds_{N2}}) \parallel (g_{m_{P6}} r_{ds_{P6}} r_{ds_{P4}})] \tag{10}$$

V. Simulation Results

The proposed CCIA has been designed in TSMC 0.18 µm process, with a single 0.6 V power supply. Cadence® Spectre simulations give a total power consumption of 683.568 nW with a total current of 1.131 29 µA. The open-loop Bode diagrams suggest a gain margin of 31 dB and a phase margin of 34^o. Fig. 7 presents the closed-loop bode of the CCIA; the gain is equal to 40.55 dB. The minimum value of the input

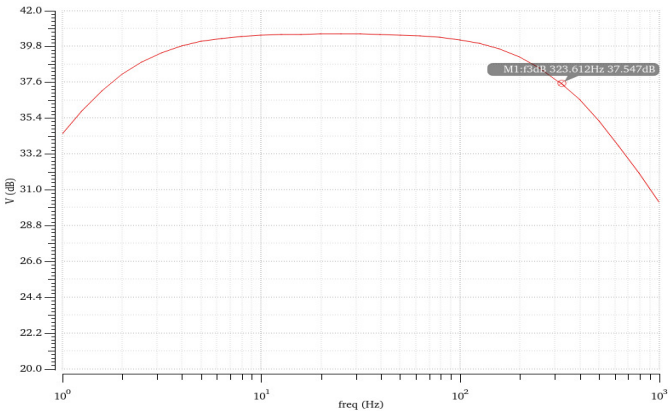

Fig. 7. CCIA closed-loop Bode diagrams.

resistance in the range 0.1 Hz-100 Hz is found to be about 270 MΩ, which is satisfactory for portable health monitoring devices.

For the chopping stabilization we choose $f_{chop} = 5$ kHz. The circuit's operation is simulated with an input of a sinusoidal wave with an amplitude of 50 µV, frequency 100 Hz and a DC offset of 50 mV to account for the EOV. Fig. 8 presents the output spectrum of the circuit. The transient behaviour of

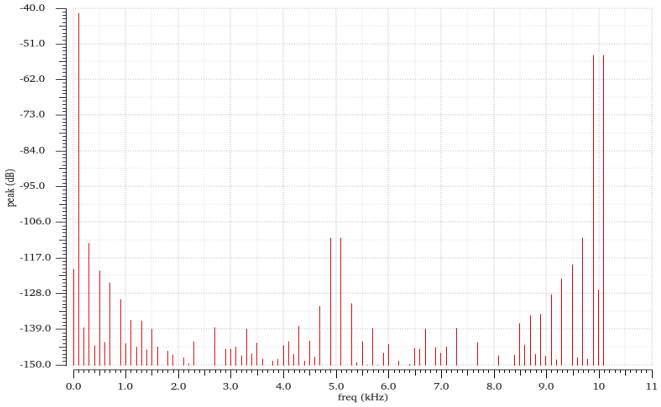

Fig. 8. Output spectrum.

the system, after the inclusion of a simple 1^{st} order differential LPF consisting of two parallel RC branches with $R = 1$ kΩ and $C = 500$ nF, is depicted in Fig.9.

The output noise PSD is shown in Fig. 10. As can be easily seen, the noise energy is concentrated at 5 kHz, and thus away from the bandwidth of interest.

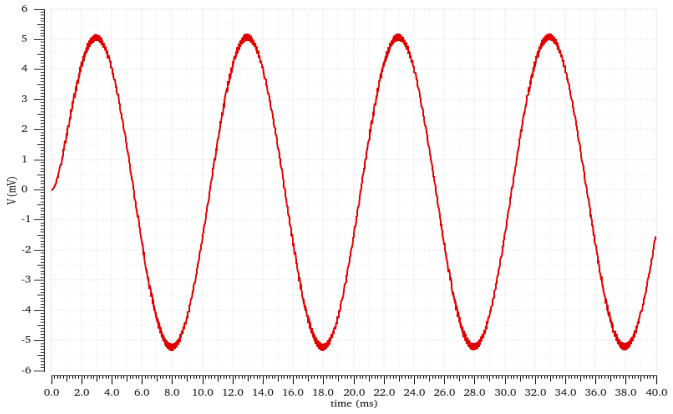

Fig. 9. Transient output after 1^{st} order LPF.

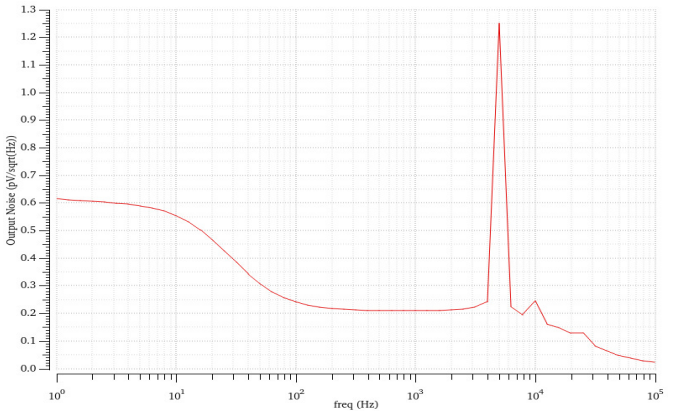

Fig. 10. Output noise PSD.

Finally, a corners analysis was run, in order to test the circuit's performance in extreme process, voltage and temperature conditions. Specifically, we test the system under a $\pm 10\%$ variation of the power supply, and for operation temperatures of $-5\,^{\circ}\mathrm{C}$ and $95\,^{\circ}\mathrm{C}$. The spurs-free dynamic range (SFDR) is highlighted in every case. The results are summarized in Table I.

TABLE I
CORNERS ANALYSIS.

Tech Model	Temp (°C)	Power Supply (mV)	SFDR dB
SS	-5	540	47.87387
SS	-5	660	68.89458
SS	95	540	54.0944
SS	95	660	66.64487
SF	-5	540	38.00138
SF	-5	660	38.71186
SF	95	540	96.25473
SF	95	660	96.42498
FS	-5	540	68.81021
FS	-5	660	69.1295
FS	95	540	75.51737
FS	95	660	90.28595
FF	-5	540	38.71437
FF	-5	660	35.70568
FF	95	540	77.923
FF	95	660	80.49634

VI. CONCLUSIONS

A CMOS capacitively-coupled instrumentation amplifier employing chopper stabilization to suppress low-frequency noise was presented. The MOSFETs composing the core of the proposed CCIA were biased in the subthreshold region, thus minimising the total power consumption. The system's simulated performance is consistent with theory, making the proposed instumentation amplifier suitable for portable health monitoring devices.

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